



PATENT ABSTRACTS OF JAPAN

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(21) Application number: **2001212073**(71) Applicant: **NEC CORP**(22) Date of filing: **12.07.01**(72) Inventor: **MATSUDA TOMOKO****(54) METHOD FOR FABRICATING SEMICONDUCTOR DEVICE**

junction leak current of an MOSFET.

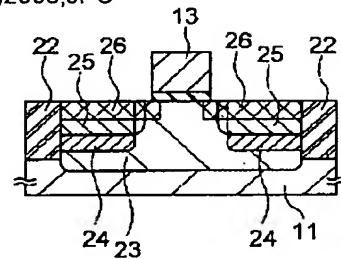
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(57) Abstract:

PROBLEM TO BE SOLVED: To provide a method for fabricating a semiconductor device in which low power consumption and high speed operation can be realized while suppressing short channel effect.

SOLUTION: When the source-drain diffusion layer of an MOSFET is formed, a gate electrode 13 having a sidewall is formed at first and In or As ions are implanted from a direction aligned with the orientation face of a substrate 1 using the gate electrode 13 as a mask thus forming a deep SD region 24 having a channeling tail of small concentration gradient in the depth direction of the substrate. Subsequently, a source-drain region 25 is formed by ordinary B or As ion implantation. The sidewall is then removed and ion implantation is performed in order to form an SD extension region 26 and a pocket region 27 before a sidewall 28 is formed again. A deep channeling tail is formed by channeling ion implantation so that a low substrate concentration can be employed thus reducing the junction capacity and

(d)



(e)

